PCI 703 Series

PCI PnP Analog Board
User's Manual

PCI703-16/A, PCI703-32/A PCI703-64/A
PCI703S-8/A, PCI703S-16/A

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Analog Boards

Data Acquisition and Process Control

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1. Introduction

The PCI703 series are 32-bit PCI bus architecture data acquisition boards. They are available in four models, the 16, 32 and 64 channels analog input board and the sample-and-hold version. The PCI703 contains digital input and output ports, onboard counters, a frequency generator, analog-in and analog-out sub-systems. The PCI703 is a multi-purpose analog board that can be used in many applications.

Features

The PCI703 does have some very unique features and are short listed below:

- 32-bit PCI bus Revision 2.2 compliant at 33MHz.
- PCI Bus 3.3V compatible.
- PCI Bus Master DMA.
- Fully individually programmable analog-in channels.
- Analog-out waveform generation support.
- Sample-and-hold option.

Feature	PCI703-XX			PCI703-XXA		
Number of analog input channels	PCI703-16	PCI703-32	PCI703-64	PCI703-16A	PCI703-32A	PCI703-64A
	16	32	64	16	32	64
Number of analog output channels	0			2		
A/D resolution @ 400 KHz	14			14		
A/D FIFO depth	4096			4096		
A/D channel list depth	4096			4096		
D/A resolution @ 100 KHz	-			14		
D/A FIFO depth	-			4096		
D/A waveform generation capability	-			YES		
Triggering capability	Internal, External. Analog & Digital. Post & Pre-Trigger			Internal, External. Analog & Digital. Post & Pre-Trigger		
Counters	3			3		
Frequency generation	1			1		
Number of digital input/output lines	8			8		
Number of multi function digital I/O lines	10			10		

Table 1-1 PCI703 16/32/64 Versions

Feature	PCI 703S-8	PCI 703S-8A	PCI 703S-16	PCI 703S-16A
Number of analog input channels	8	16	16	16
Number of analog output channels	0	2	0	2
A/D resolution @ 400 KHz	14		14	14
A/D FIFO depth	4096	4096	4096	4096
A/D channel list depth	4096	4096	4096	4096
D/A resolution @ 100 KHz	-	14	-	14
D/A FIFO depth	-	4096	-	4096
D/A waveform generation capability	-	YES	-	YES
Triggering capability	Internal, External. Analog & Digital. Post & Pre-Trigger	Internal, External. Analog & Digital. Post & Pre-Trigger	Internal, External. Analog & Digital. Post & Pre-Trigger	Internal, External. Analog & Digital. Post & Pre-Trigger
Counters	3	3	3	3
Frequency generation	1	2	1	1
Number of digital input/output lines	8	8	8	8
Number of multi function digital I/O lines	10	10	10	10

Table 1-2 PCI703S Versions

Applications

The PCI703 can be used in the following applications:

- Vibration monitoring.
- Transducer monitoring.
- Automation and test equipment.
- Signal generation.
- Laboratory training.
- Medical applications.

Key Specifications

- 14-bit analog input @ 400 KHz.
- Fully programmable sample-and-hold analog input system with triggering.
- 14-bit analog output @ 400 KHz.
- Independent waveform generation capability.

Software Support

The PCI703 is supported by EDR Enhanced and comes with an extensive range of examples. The software will help you to get your hardware going very quickly. It also makes it easy to develop complicated control applications quickly. All operating system drivers, utility and test software are supplied on the Eagle Technology CD-Rom. The latest drivers can also be downloaded from the Eagle Technology website. For further support information see the Contact Details section.

Contact Details

Below are the contact details of Eagle Technology.

Eagle Technology
PO Box 4376
Cape Town
8000
South Africa
Telephone +27 (021) 423 4943
Fax +27 (021) 424 4637
E-Mail eagle@eagle.co.za
Website http://www.eagledaq.com

2

2. Installation

This chapter describes how to install and configure the PCI703 for the first time. Minimal configuration is necessary; almost all settings are done through software. The PCI BIOS or operating system will take care of all resource assignments.

Package

PCI703 package will contain the following:

- PCI703 PCI board
- Software CD-Rom

Operating System Support

PCI703 support the following operating systems

Board Type	Revision	Operating Systems	Driver Type
PCI703-16/A	Revision 1	Windows NT/2000	NT Sys
PCI703-16/A	Revision 2	Windows NT/2000/98/ME	NT Sys, WDM PnP
PCI703-64/A	Revision 2	Windows NT/2000/98/ME	NT Sys, WDM PnP
PCI703S-8/16/A	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP

Table 2-1 Operating System Support

Hardware Installation

This section will describe how to install your PCI board into your computer.

- Switch off the computer and disconnect from power socket.

Failure to disconnect all power cables can result in hazardous conditions, as there may be dangerous voltage levels present in externally connected cables.

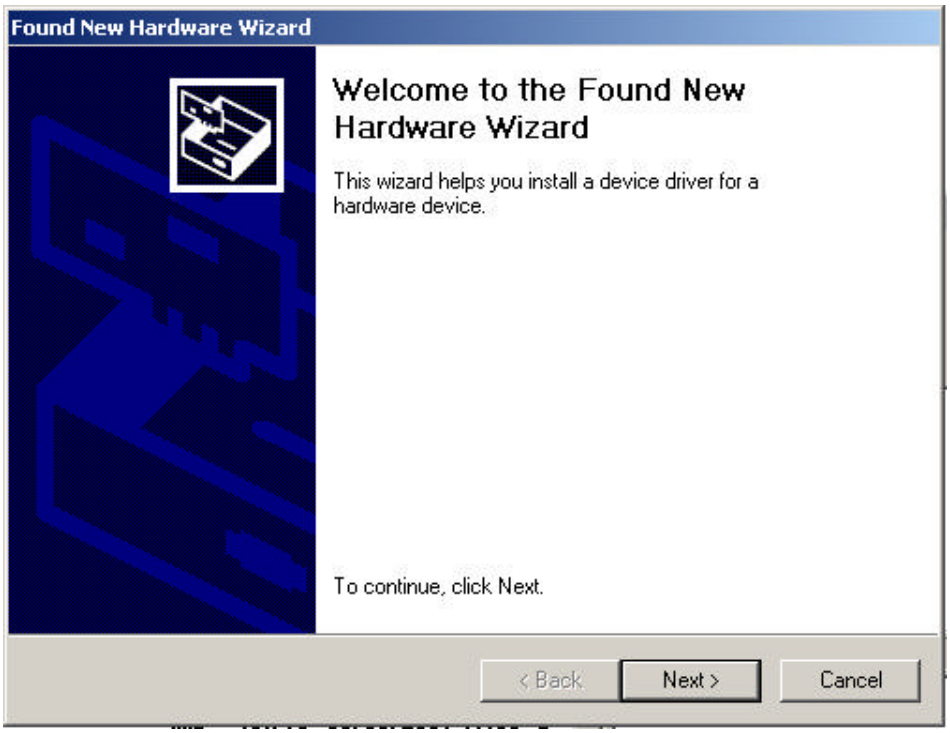
- Remove the cover of the PC.
- Choose any open PCI slot and insert PCI board
- Insert bracket screw and ensure that the board sits firmly in the PCI socket.
- Replace the cover of the PC.
- Reconnect all power cables and switch the power on.
- The hardware installation is now completed.

Software Installation

Windows 98/2000/ME

Installing the Windows 98/2000 device driver is a very straightforward task. Because it is plug and play Windows will auto detect the PCI board as soon as it is installed. No setup is necessary. You simply have to supply Windows with a device driver.

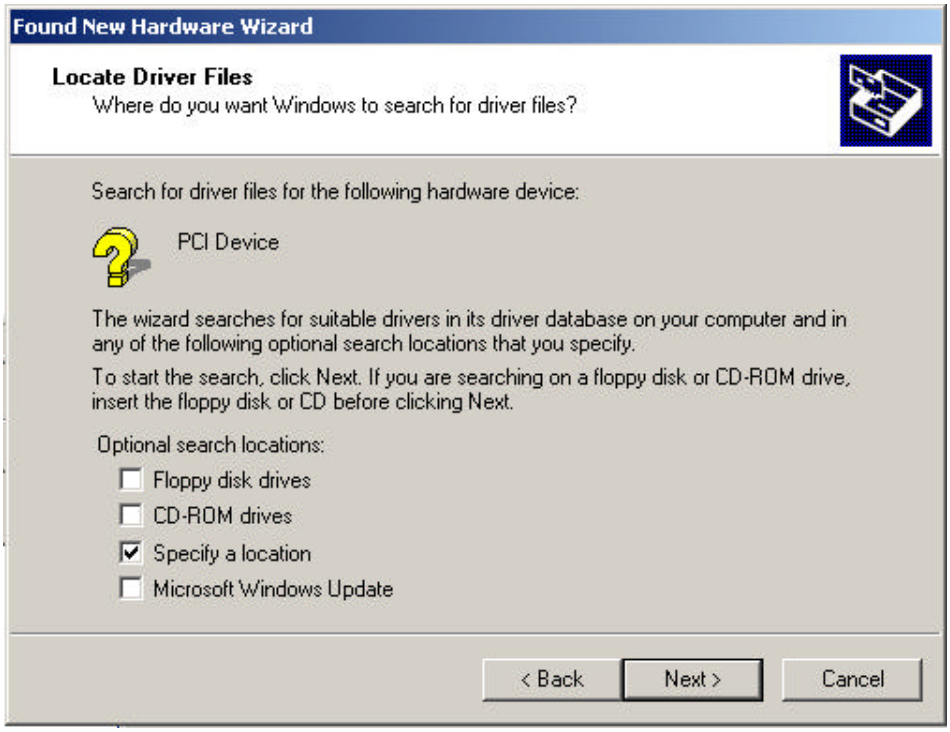
Wait until Windows detects the new hardware


Found New Hardware Wizard
Welcome to the Found New Hardware Wizard
This wizard helps you install a device driver for a hardware device.
To continue, click Next.
< Back
Next >
Cancel

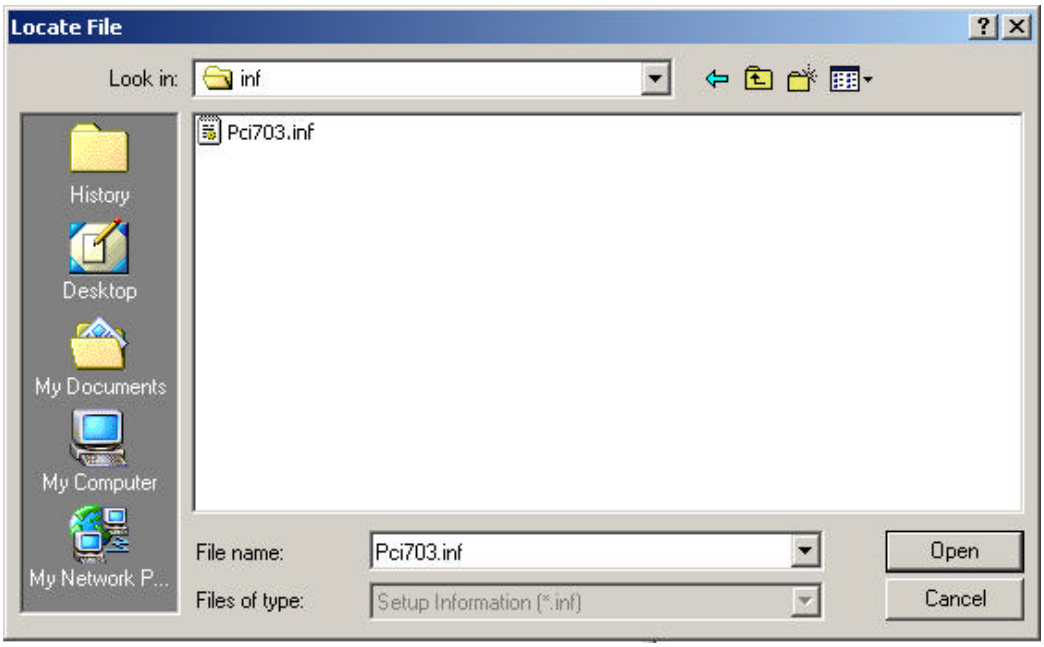
Select Next

Found New Hardware Wizard
Install Hardware Device Drivers
A device driver is a software program that enables a hardware device to work with an operating system.
This wizard will complete the installation for this device:
PCI Device
A device driver is a software program that makes a hardware device work. Windows needs driver files for your new device. To locate driver files and complete the installation click Next.
What do you want the wizard to do?
Search for a suitable driver for my device (recommended)
Display a list of the known drivers for this device so that I can choose a specific driver
< Back
Next >
Cancel

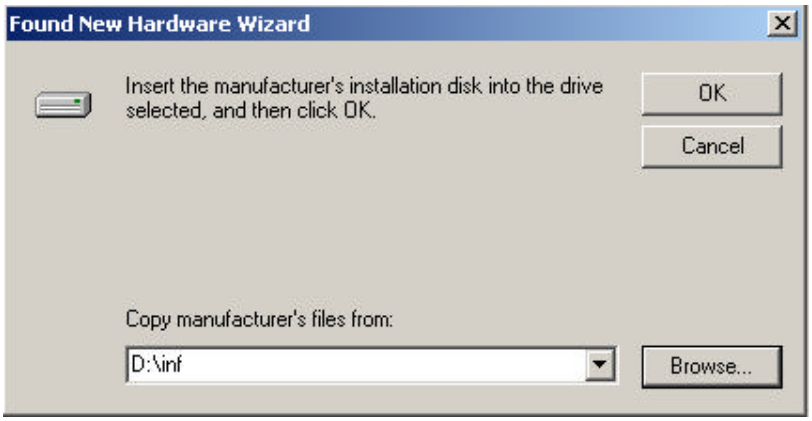
Select "Search for a suitable driver for my device…" and select next


Found New Hardware Wizard
Locate Driver Files
Where do you want Windows to search for driver files?
Search for driver files for the following hardware device:
PCI Device
The wizard searches for suitable drivers in its driver database on your computer and in any of the following optional search locations that you specify.
To start the search, click Next. If you are searching on a floppy disk or CD-ROM drive, insert the floppy disk or CD before clicking Next.
Optional search locations:
Floppy disk drives
CD-ROM drives
Specify a location
Microsoft Windows Update
< Back
Next >
Cancel

Make sure only "Specify a location" is selected and select next



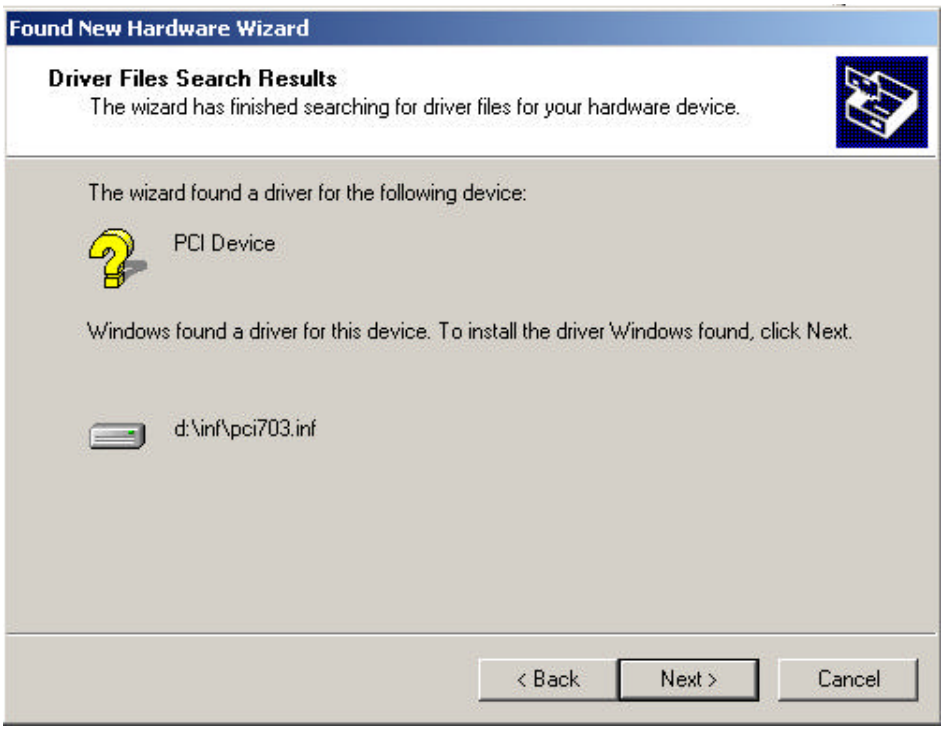
Select the browse button and search for the PCI703.inf file on the Eagle CD-Rom.



The driver is normally located in the <CDROM>:\EDRE\DRIVERS\WDM\PCI703 directory.

The PCI703/16/64 use the same driver. However the PCI703S has a different driver. Please sure that you use the appropriate driver for your board.

Select next when found.


Found New Hardware Wizard
Driver Files Search Results
The wizard has finished searching for driver files for your hardware device.
The wizard found a driver for the following device:
PCI Device
Windows found a driver for this device. To install the driver Windows found, click Next.
d:\inf\pci703.inf
< Back
Next >
Cancel

Select next again.

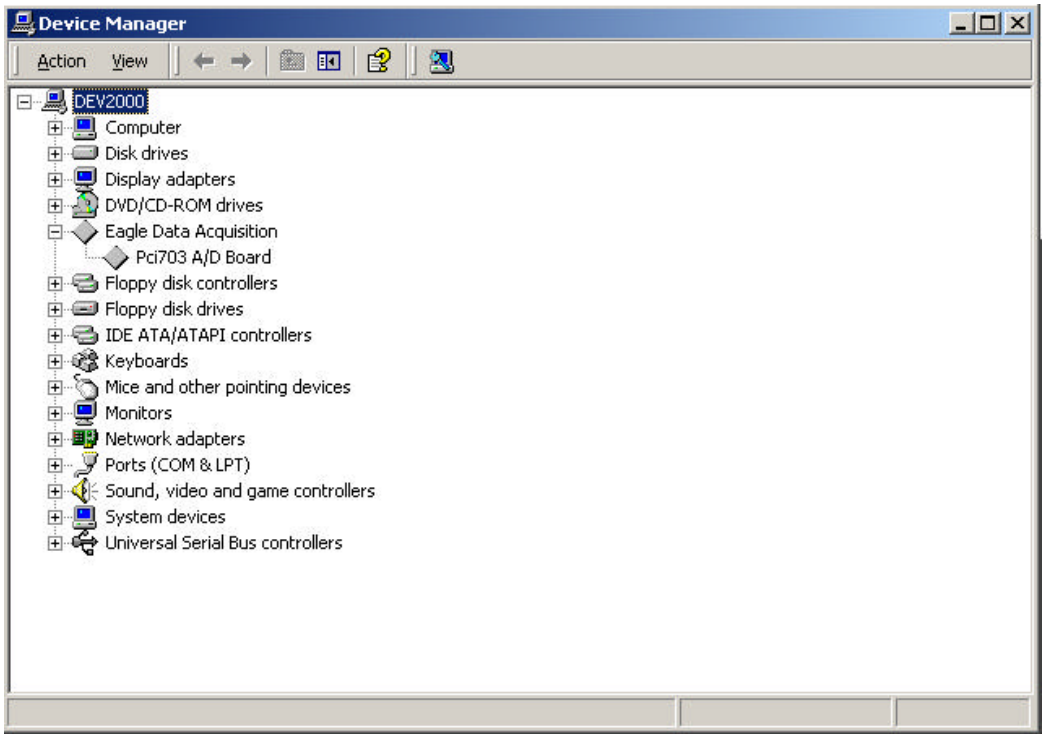
Found New Hardware Wizard
Completing the Found New Hardware Wizard
Pci703 A/D Board
Windows has finished installing the software for this device.
To close this wizard, click Finish.
< Back
Finish
Cancel

When done you might have to restart your computer.

Post installation

When done with the driver installation the device manager can be open to make sure the installation was a success.

- First make sure that the driver is working properly by opening the *Device Manager*.
- Check under the Eagle Data Acquisition list if your board is listed and working properly. See picture below.



- Clearly you can see that the PCI device is listed and working properly.
- Further open the control panel and then the *EagleDAQ* folder. This dialog should list all installed hardware. Verify your board's properties on this dialog. See picture below

Now the first part of your installation has been completed and ready to install the EDR Enhanced Software Development Kit.

- Run ***edreapi.exe*** found on the Eagle CD-Rom and follow the on screen instructions

Windows NT

Windows NT does not require any special setup procedure. The Windows NT driver does not support plug and play. If Windows 2000 detects a new device simply install a default driver, or so called placeholder. This will disable the device in the plug and play manager.

To install the Windows NT drivers simply run ***edrewinnt.exe*** on the Eagle CD-Rom. This will automatically install the device drivers. Restart your computer when done. Open the *EagleDAQ* folder in the control panel to check if your installation was successful.

Accessories

The PCI703 has got a wide variety of accessories that it can be connected too. See the Eagle Technology catalog for more information.

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3. Interconnections

The PCI703 has got one external connector that includes connections for analog-in, analog-out, digital I/O, counters and power. All connections are made through this connector situated on the card's bracket.

A wide variety of genuine accessories available from Eagle Technology also make interfacing to the PCI703 very easy. Accessories are available in the form of cables, screw terminals and application modules.

External Connectors

PCI703-16/A

The PCI703-16/A has a SCSI male centronics 68-way connector. Two types of cables are available, 68-way SCSI-II D-Sub (F) to (M) screened cable connecting to an adaptor ADPT6868 and a Y-Cable 68-way SCSI-II D-Sub (F) to 2 x DB37 (F) connection to application modules and adaptors. Application modules include the PC43A4 and PC52A1. Adaptors would be the ADPT3740. See diagram below.

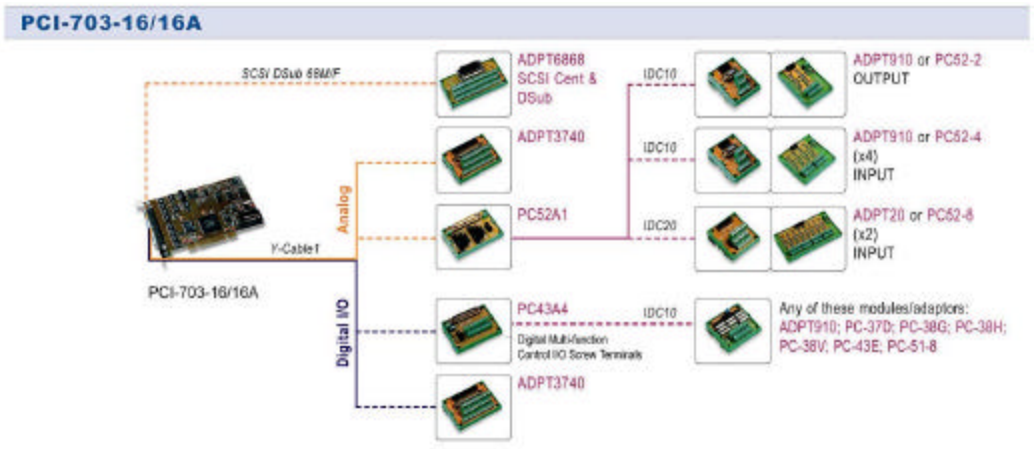


Figure 3-A PCI 703 Interconnections

Connector Pin Assignments

PCI703-16/A

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	FREQ_OUT	18	DGND	35	DGND	52	DIO0
2	GPCTR0	19	DIO4	36	DGND	53	DGND
3	PFI9	20	RESERVED	37	PFI8/ CPCTR1	54	AOGND
4	DGND	21	DAC1	38	PFI7	55	AOGND
5	PFI6	22	DAC0	39	DGND	56	AIGND
6	PFI5	23	ACH15	40	GPCTR1	57	ACH7
7	DGND	24	AIGND	41	PFI4	58	ACH14
8	+5V	25	ACH6	42	PFI3/CPCTR0	59	AIGND
9	DGND	26	ACH13	43	PFI2/CONVERT	60	ACH5
10	PFI1	27	AIGND	44	DGND	61	ACH12
11	PFI0/TRIG1	28	ACH4	45	RESERVED	62	AISENSE
12	DGND	29	AIGND	46	SCANCLK	63	ACH11
13	DGND	30	ACH3	47	DIO3	64	AIGND
14	+5V	31	ACH10	48	DIO7	65	ACH2
15	DGND	32	AIGND	49	DIO2	66	ACH9
16	DIO6	33	ACH1	50	DGND	67	AIGND
17	DIO1	34	ACH8	51	DIO5	68	ACH0

Table 3-1 Pinouts for PCI703-16/A (External Connector – SCSI 68)

The following cables can be used with this connector.

- Y-Cable 1
- SCSI D-Sub 68 M/F

PCI703-32/64/A

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AIGND	26	DIO4	51	ACH16	76	AIGND
2	AIGND	27	DIO1	52	ACH24	77	ACH36
3	ACH0	28	DIO5	53	ACH17	78	ACH44
4	ACH8	29	DIO2	54	ACH25	79	ACH37
5	ACH1	30	DIO6	55	ACH18	80	ACH45
6	ACH9	31	DIO3	56	ACH26	81	ACH38
7	ACH2	32	DIO7	57	ACH19	82	ACH46
8	ACH10	33	DGND	58	ACH27	83	ACH39
9	ACH3	34	+5V	59	ACH20	84	ACH47
10	ACH11	35	+5V	60	ACH28	85	ACH48
11	ACH4	36	SCANCLK	61	ACH21	86	ACH56
12	ACH12	37	EXTSTROBE	62	ACH29	87	ACH49
13	ACH5	38	PFI0/TRIG1	63	ACH22	88	ACH57
14	ACH13	39	PFI1	64	ACH30	89	ACH50
15	ACH6	40	PFI2/CONVERT	65	ACH23	90	ACH58
16	ACH14	41	PFI3/ CPCTR0	66	ACH31	91	ACH51
17	ACH7	42	PFI4	67	ACH32	92	ACH59
18	ACH15	43	GPCTR1	68	ACH40	93	ACH52
19	AISENSE	44	PFI5/UPDATE	69	ACH33	94	ACH60
20	DAC0OUT	45	PFI6/WFTRIG	70	ACH41	95	ACH53
21	DAC1OUT	46	PFI7/STARTSCAN	71	ACH34	96	ACH61
22	EXTREF	47	PFI8/ CPCTR1	72	ACH42	97	ACH54
23	AOGND	48	PFI9	73	ACH35	98	ACH62
24	DGND	49	GPCTR0	74	ACH43	99	ACH55
25	DIO0	50	FREQ_OUT	75	AISENSE	100	ACH63

Table 3-2 Pinouts for PCI703-32/64/A (External Connector – SCSI 100)

The following cable can be used with this connector

- Y-Cable 3
- SCSI D-Sub 100 M/M

PCI703S-8/16/A

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AIGND	18	ACH0+	35	AIGND	52	ACH1+
2	ACH14-	19	DAC0	36	ACH15-	53	DAC1
3	ACH14+	20	AOGND	37	ACH15+	54	AOGND
4	ACH12-	21	DGND	38	ACH13-	55	DGND

5	ACH12+	22	FREQ_OUT	39	ACH13+	56	NC
6	ACH10-	23	GPCTR0	40	ACH11-	57	GPCTR1
7	ACH10+	24	PFI8/ CPCTR1	41	ACH11+	58	PFI9
8	ACH8-	25	PFI6	42	ACH9-	59	PFI7/STARTSCAN
9	ACH8+	26	PFI4	43	ACH9+	60	PFI5
10	AIGND	27	PFI2/CONVERT	44	AIGND	61	PFI3/ CPCTR0
11	ACH6-	28	PFI0/TRIG1	45	ACH7-	62	PFI1
12	ACH6+	29	+5V	46	ACH7+	63	+5V
13	ACH4-	30	DGND	47	ACH5-	64	DGND
14	ACH4+	31	DIO6	48	ACH5+	65	DIO7
15	ACH2-	32	DIO4	49	ACH3-	66	DIO5
16	ACH2+	33	DIO2	50	ACH3+	67	DIO3
17	ACH0-	34	DIO0	51	ACH1-	68	DIO1

Table 3-3 Pinouts for PCI703S-8/16/A (External Connector – SCSI 68)

The following cable can be used with this connector.

- SCSI D-Sub M/F-S
- Y-Cable 4

Cable Pin Assignments

Y–Cable 1 (PCI 703-16/A) Analog –DB37 F

Pin	Name	Pin	Name
1	AIGND	20	ACH0
2	ACH1	21	AIGND
3	ACH2	22	ACH3
4	AIGND	23	ACH4
5	ACH5	24	AIGND
6	ACH6	25	ACH7
7	AIGND	26	ACH8
8	ACH9	27	AIGND
9	ACH10	28	ACH11
10	AIGND	29	ACH12
11	ACH13	30	AIGND
12	ACH14	31	ACH15
13	AIGND	32	AISENSE
14	AIGND	33	NC
15	NC	34	NC
16	AOGND	35	EXTREF
17	AOGND	36	DAC0
18	AOGND	37	DAC1
19	AOGND		

Table 3-4 Y-Cable 1 Analog Connector

Y-Cable 3 (PCI 703-64/A) Analog

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AIGND	21	ACH32	41	AIGND	61	ACH40
2	ACH0	22	ACH33	42	ACH8	62	ACH41
3	ACH1	23	ACH34	43	ACH9	63	ACH42
4	ACH2	24	ACH35	44	ACH10	64	ACH43
5	ACH3	25	ACH36	45	ACH11	65	ACH44
6	ACH4	26	ACH37	46	ACH12	66	ACH45
7	ACH5	27	ACH38	47	ACH13	67	ACH46
8	ACH6	28	ACH39	48	ACH14	68	ACH47
9	ACH7	29	AIGND	49	ACH15	69	AIGND
10	ANALOG I/P SENSE	30	ACH48	50	AAIGND	70	ACH56
11	AIGND	31	ACH49	51	ANALOG I/P SENSE	71	ACH57
12	ACH16	32	ACH50	52	ACH24	72	ACH58
13	ACH17	33	ACH51	53	ACH25	73	ACH59
14	ACH18	34	ACH52	54	ACH26	74	ACH60
15	ACH19	35	ACH53	55	ACH27	75	ACH61
16	ACH20	36	ACH54	56	ACH28	76	ACH62
17	ACH21	37	ACH55	57	ACH29	77	ACH63
18	ACH22	38	AOGND	58	ACH30	78	AOGND
19	ACH23	39	DAC0	59	ACH31	79	DAC1
20	AIGND	40	AOGND	60	AIGND	80	EXTREF

Table 3-5 Y-Cable 3 Analog Connector

Y–Cable 1, Y-Cable 3, Y-Cable 4 (PCI 703-16/64/S/A) Digital –DB37 F

Pin	Name	Pin	Name
1	DGND	20	DIO0
2	DIO1	21	DGND
3	DIO2	22	DIO3
4	DGND	23	DIO4
5	DIO5	24	DGND
6	DIO6	25	DIO7
7	DGND	26	+5V
8	DGND	27	SCANCLK
9	EXTSTROBE	28	PFI0/TRIG1
10	DGND	29	+5V
11	DGND	30	PFI1
12	PFI2/CONVERT	31	PFI3
13	DGND	32	PFI4
14	PFI5	33	PFI6
15	DGND	34	GPCTR1
16	PFI7	35	PFI8
17	DGND	36	PFI9
18	GPCTR0	37	FREQ_OUT
19	GND		

Table 3-6 Y-Cable 1,3,4 Digital Connector

Signal Definitions

This sections deal with all the signals abbreviations.

Signal	Description
ACH0-63	Analog inputs
AIGND	Analog input ground
AOGND	Analog output ground
AISENSE	Analog input sensing
DAC0-1	Analog outputs
DIO0-7	Digital inputs/outputs
PFI0-9	Programmable multi function digital inputs/outputs
TRIG1	Digital trigger pin
FREQ_OUT	Frequency generator
SCANCLK	A/D external convert
GPCTR0-1	Counter Outputs
CPCTR0-1	Counter Inputs
+5V	Power output
DGND	Digital ground

Table 3-2 Signal definitions

Pin Descriptions

Analog Input (ACH0-63)

This is the analog input-channels. Depending on the version there are either 16/64 single ended input channels or 8/32 differential input channels.

Analog Input Sensing (AISENSE)

This input is used as a reference analog input ground. This is normally used where the measurement point is very far from the PCI703 connector.

Analog Input Ground (AIGND)

This is the analog reference used by single ended analog inputs.

Analog Output Ground (AOGND)

This is the analog reference used by analog outputs.

Analog Outputs (DAC0-1)

The A version of the PCI703 has two analog outputs, DAC0 and DAC1.

Digital Input/Outputs (DIO0-7)

The DIO0-7 pins are the pins for the digital I/O system.

Multi Function Digital Input/Outputs (PIO0-7)

These pins are digital I/O, but can also be used for some other functions. Th ey represent the same function as the digital I/O pins.

TRIG1

This pin is used for digital triggering.

Frequency Output (FREQ_OUT)

This is the output pin of the frequency generator system.

ADC Scan Clock (SCANCLK)

This input is used to externally clock the ADC system.

Counters Output (GPCTR0-1)

These are the outputs of the two user counters.

Counters External Clock (CPCTR0-1)

These are the external clock inputs of the two user counters.

+5V Power Pin (+5V)

This is a +5 volt fused power pin.

Digital Ground (DGND)

All digital ground signals should be connected to this pin.

Analog Input Connections

WARNING!!

All unused analog inputs must be connected to analog ground. The analog input system of the PCI703 can be damaged or become unstable when scanning channels that is left floating.

Analog Input Connections - SAMPLE-AND-HOLD

WARNING!!

Don't feed any voltage into the PCI703S while the computer is switched off. This will damage the analog input cicuitry. The sample-and-hold devices will be damaged parmanently and result in multfunctioning of the board.

Differential Input Pairing

The table below shows the differential channel pairing. This is for the PCI703-16/32/64 boards. Please note that if any channel is assigned as a differential input, the paired channel will automatically become unavailable. The positive channel is the channel that needs to be configured.

Channel Number	Positive Channel	Negative Channel	Channel Number	Positive Channel	Negative Channel
0	0	8	16	32	40
1	1	9	17	33	41
2	2	10	18	34	42
3	3	11	19	35	43
4	4	12	20	36	44
5	5	13	21	37	45
6	6	14	22	38	46
7	7	15	23	39	47
8	16	24	24	48	56
9	17	25	25	49	57

10	18	26	26	50	58
11	19	27	27	51	59
12	20	28	28	52	60
13	21	29	29	53	61
14	22	30	30	54	62
15	23	31	31	55	63

Table 3-7 Differential Channel Assignment

4

4. Programming Guide

The PCI703 is supplied with a complete software development kit. EDR Enhanced (EDRE SDK) comes with drivers for many operating systems and a common application program interface (API). The API also serves as a hardware abstraction layer (HAL) between the control application and the hardware. The EDRE API makes it possible to write an application that can be used on all hardware with common sub-systems.

The PCI703 can also be programmed at register level, but it is not recommended. A detailed knowledge of the PCI703 is needed and some knowledge about programming Plug and Play PCI devices. We recommend that you only make use of the software provided by Eagle Technology.

EDR Enhanced API

The EDR Enhanced SDK comes with both ActiveX controls and a Windows DLL API. Examples are provided in many different languages and serve as tutorials. EDRE is also supplied with a software manual and user's guide.

The EDRE API hides the complexity of the hardware and makes it really easy to program the PCI703. It has got functions for each basic sub-system and is real easy to learn.

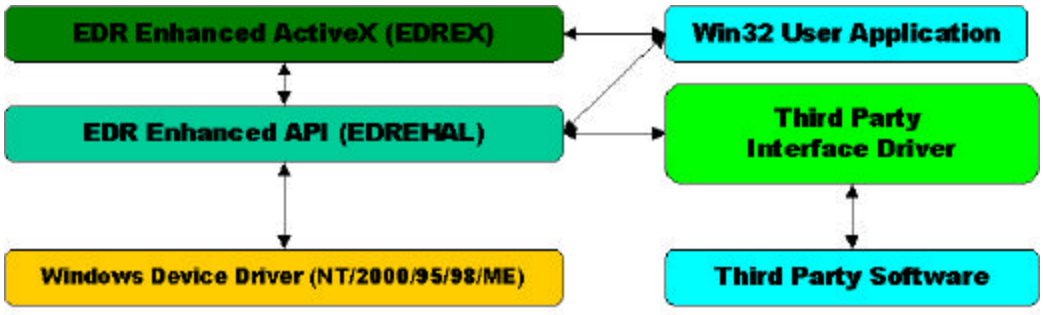


Figure 4-A EDR Enhanced Design

Digital Inputs/Outputs

The PCI703 has got 8 digital I/O lines and 10 multi I/O lines that can all be used for digital control purposes. The EDRE API supports auto direction configuration. By writing to or reading from a port, it is automatically configured as an output or input. A port is defined as a collection of simultaneous configurable entities. Thus in the case of the PCI703 each port is only 1-bit wide. In total the PCI703 has got 18 digital ports that can be configured in any direction. Some of which has got more than one function when configured as an input.

Reading the Digital Inputs

A single call is necessary to read a digital I/O port.

API-CALL

Long EDRE_DioRead(ulng Sn, ulng Port, ulng *Value)

The serial number, port, and a pointer to variable to hold the result must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Read(long Port)

Only the port-number needs to be passed and the returned value will either hold an error or the value read. If the value is negative an error did occur.

Writing to the Digital Outputs

A single call is necessary to write to a digital I/O port.

API-CALL

Long EDRE_DioWrite(ulng Sn, ulng Port, ulng Value)

The serial number, port, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Write(long Por, ulng Value)

The port number and value to be written needs to be passed and the returned value holds an error or the value read. If the value is negative an error did occur.

Counters

The counter sub-system is supported by functions to Write, Configure and controlling the gate. There are 3 counters and 1 frequency generator. Only the first two counters and the frequency generator are available for the user. See the table below that shows the relation of the counters and their assigned numbers.

Counter	Assigned Number	Description
0	0	Counter 0
1	1	Counter 1
2	<Not Used>	A/D Timing
3	2	Frequency Out Counter

Table 4-1 Counter Assignment

Writing the initial counter value

A single call is necessary to write a counter's initial load value.

API-CALL
Long EDRE_CTWrite(ulng Sn, ulng Ct, ulng Value)
The serial number, counter-number, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL
Long EDRECTX.Write(long Port, ulng Value)
The port number and value to be written needs to be passed and the returned value holds an error or the value read. If the value is negative an error did occur.

Configuring a counter

A single call is necessary to configure a counter.

API-CALL
Long EDRE_CTConfig(ulng Sn, ulng Ct, ulng Mode, ulng Type, ulng ClkSrc, ulng GateSrc)
The serial number, counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

ACTIVEX CALL
Long EDRECTX.Configure(long ct, long mode, long type, ulng source, ulng gate)
The counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

Only the counter mode, clock source and type parameters are used by the PCI703. The table below shows the options for each parameter.

Parameter	Description
Sn	Serial Number
Ct	Counter Number: 0 : Counter 0 1 : Counter 1 2 : Frequency Out Counter
Mode	0 : PULSE 1 : TOGGLE Invalid parameter for counter 2
Type	Interrupt on TC: 0 : Disabled 1 : Enabled This bit will only generate a interrupt at the interrupt sub-system. The interrupt sub-system must also be setup to generate a PCI Bus interrupt.
Source	0 : 20MHz internal clock 1 : 100KHz internal clock 2 : External clock on CPCTRx pin<invalid for counter 2>

Gate	<not use>

Table 4-2 Counter Configuration

Controlling the counter gate

A single call is necessary to setup/control a counter's gate. This function call is invalid for the frequency generator (counter 2). Counter 2 does not have a gate.

API-CALL
Long EDRE_CTSoftGate(ulng Sn, ulng Ct, ulng Gate)
The serial number, counter-number and gate are needed to control a counter's gate. A return code will indicate if any errors occurred.

ACTIVEX CALL
Long EDRECTX.SoftGate(ulng Sn, ulng Ct, ulng Gate)
The counter-number and mode is needed to control a counter's gate. A return code will indicate if any errors occurred.

These values are acceptable as a gate source.

Value	Description
0	Gate disabled
1	Gate enabled

Table 4-3 Gate Configuration

Analog Output

The PCI703-X/A version has got 2 DAC channels that support single write and waveform generation. The DAC subsystem uses the onboard counters for timing and a FIFO for data transfer. The two DAC channels are controlled independently from each other. The DAC subsystem is control via 3 functions: SingleWrite, Control and Configure.

Writing to a DAC channel

A single call is necessary to set a voltage on a DAC channel.

API-CALL

Long EDRE_DAWrite (ulng Sn, ulng Channel, long uVoltage)

The serial number, DAC channel and micro-voltage is needed to set a DAC channel's voltage. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDAX.Write (ulng Channel, long uVoltage)

The DAC channel and micro-voltage is needed to set a DAC channel's voltage. A return code will indicate if any errors occurred.

Generating a Waveform

Generating a waveform is basically a two-step process. First configure a channel then start and stop it. Two modes are available, FIFO non-loop mode and pattern mode. FIFO non-loop the FIFO data only gets outputted once. The DAC output voltage will be the same as the last value in the FIFO. In pattern mode the FIFO data is outputted continuously. Please note that the frequency is not the total frequency of the waveform, but the update rate of the DAC channel. This is the value written directly to the counter.

Update frequency = (Internal clock frequency) / (counter value +1)

API-CALL

Long EDRE_DAConfig (ulng Sn, ulng Channel, ulng Frequency, ulng ClkSrc, ulng GateSrc, ulng Continuous, ulng Length, long *uVoltage)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Channel	Unsigned long	Channel 0: DAC Channel 0 1: DAC Channel 1
Frequency	Unsigned long	Actual value written to counter
ClkSrc	Unsigned long	Clock source 0: Internal 20 MHz 1: Internal 100 KHz 2: External Clock
GateSrc	Unsigned long	Gate Source – Ignored
Continuous	Unsigned long	Mode 0: NON LOOP MODE 1: LOOP MODE
Length	Unsigned long	Buffer length
uVoltage	Pointer to a long buffer	Buffer filled with micro voltages
Return	Long	Error Code

ACTIVEX CALL

Long EDRDAX.Configure (long Channel, long Frequency, long ClkSrc, long GateSrc, long Continuous, long Length, long *uVoltage)

Parameter	Type	Description

Channel	Long	Channel 0: DAC Channel 0 1: DAC Channel 1
Frequency	Long	Actual value written to counter
ClkSrc	Long	Clock source 0: Internal 20 MHz 1: Internal 100 KHz 2: External Clock
GateSrc	Long	Gate Source – Ignored
Continuous	Long	Mode
Length	Long	Number of samples in buffer
uVoltage	Pointer to a long buffer	Buffer filled with micro voltages
Return	Long	Error Code

API-CALL
Long EDRE_DAControl (ulng Sn, ulng Channel, ulng Command)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Channel	Unsigned long	Channel 0: DAC Channel 0 1: DAC Channel 1
Command	Unsigned long	Command Code 0: NULL 1: Start process 2: Stop process 3: Pause process 4: Continue process
Return	Long	Error Code

ACTIVEX CALL
Long EDREDAX.Control (long Channel, long Command)

Parameter	Type	Description
Channel	Long	Channel 0: DAC Channel 0 1: DAC Channel 1
Command	Long	Command Code 0: NULL 1: Start process 2: Stop process 3: Pause process 4: Continue process
Return	Long	Error Code

Analog Input

The PCI703 has got a very unique A/D subsystem and is fully configurable. Configuration includes dynamic range, gain, reference and differential or single ended. Each of these settings can be applied to an individual channel while scanning.

Please not that although the PCI703 and PCI703S is similar in operation and uses the same functions, not all parameters apply to the PCI703S. This is because the PCI703S only supports bipolar-differential mode. The frequency is also implemented differently. Where the frequency is the timer tic for the ADC on the PCI703, it is the total frequency on the PCI703S.

Reading a single voltage from a channel

To read a single ADC channel you need to know the voltage range and gain.

API-CALL
Long EDRE_ADSingle (ulng Sn, ulng Channel, ulng Gain, ulng Range, plong uVoltage)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Channel	Unsigned long	ADC Channel
Gain	Unsigned long	Gain code. See appendix for details
Range	Unsigned long	Range code. See appendix for details
uVoltage	Pointer to a long	Voltage read from channel
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.SingleRead (long Channel)

Parameter	Type	Description
Channel	Long	ADC Channel
Return	Long	Voltage returned from channel.

Make sure to set the *Gain* and *Range* properties of the ADC ActiveX control. This will in turn set the range and gain when reading the ADC channel.

Configuring the ADC subsystem for scanning

This is the most complicated part of configuring the PCI703 for auto scanning. Make sure that you use the correct format when applying the channel list configuration. There are many loopholes and care should be taken when implementing code to configure the PCI703.

API-CALL
Long EDRE_ADConfig (ulng Sn, pulng Freq, ulng ClkSrc, ulng Burst, ulng Range, pulng ChanList, pulng GainList, ulng ListSize)

The following parameters must be specified when configuring the ADC sub-system.

<table>
<tr><th>Parameter</th><th>Type</th><th>Description</th></tr>
<tr><td>Sn</td><td>Unsigned long</td><td>Board's serial number.</td></tr>
<tr><td>Freq</td><td>Pointer to an unsigned long</td><td>Sampling frequency. The actual sampling frequency will be returned with this parameter.</td></tr>
<tr><td>ClkSrc</td><td>Unsigned long</td><td>This parameter is used to configure the clocking system of the ADC.
Format
<table>
<tr><th>Offset (bits)</th><th>Description</th></tr>
<tr><td>0</td><td>Clock Source (C0-C7)
0: Undefined
1: Internal
2: External – PIN PFI2/CONVERT</td></tr>
<tr><td>8</td><td>Trigger Source (T0-T3)
0: Internal
1: Reference – DAC CHAN 1 (NOT SUPPORTED BY PCI 703S)
2: External – PIN TRIG1</td></tr>
</table>
</td></tr>
</table>

		12 — Trigger Mode – Only applies to the reference trigger source. (M0-M3) 0: Positive 1: Negative 2: Rising 3: Falling

Example Layout:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M3	M2	M1	M0	T3	T2	T1	T0	C7	C6	C5	C4	C3	C2	C1	C0

Burst	Unsigned long	Not used
Range	Unsigned long	Not used
ChanList	Pointer to an unsigned long	This is an array of unsigned longs which contains the channels to be sampled when scanning the ADC sub-system. The max size of the channel list is half the FIFO depth.
GainList	Pointer to an unsigned long	The gain list contains an array of unsigned longs which sp ecifies the setup for each channel according to the previous list. The table below shows the format for each channel.

Offset (bits)	Description
0	Specifies the gain of the channel. See table on ADC gain codes. (G)
8	Specifies the range of the channel. Se e table on ADC range codes. (R)
12	Specifies the analog reference. 0: analog in sense pin. 1: analog ground. (F)

Example Layout:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F3	F2	F1	F0	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0

ListSize	Unsigned long	This parameter determines the length the two previous arrays. This is also the depth of the channel list that is programmed to the board.

Digital triggering

If digital triggering is used, pin TRIG1 is used. This pin is active high and will start the ADC process when it is high. The process will continue until it is stopped via software.

Analog triggering

If analog triggering is used, the voltage on analog output channel 1 is used as reference voltage. This voltage can be changed at set and the PCI703 will compare the current input voltage to the ADC system, this can be from any channel included in the channel list, with the voltage of DAC channel 1. The trigger event can be any of the four settings.

ACTIVEX CALL

Long EDREADX.Configure (plong Channels, plong Gains, long ListSize)

Parameter	Type	Description
Channels	Pointer to a long	This is an array of longs that contains the channels to be sampled when scanning the ADC sub-system. The max size of the channel list is half the FIFO depth.
Gains	Pointer to a long	The gain list contains an array of longs that specifies the setup for each channel according to the previous list. The table below shows the format for each channel.

Offset (bits)	Description
0	Specifies the gain of the channel. See table on ADC gain codes. (G)
8	Specifies the range of the channel. See table on ADC range codes. (R)
12	Specifies the analog reference. 0: analog in sense pin.

Example Layout:

		F3 F2 F1 F0 R3 R2 R1 R0 G7 G6 G5 G4 G3 G2 G1 G0
ListSize	Unsigned long	This parameter determines the length the two previous arrays. This is also the depth of the channel list that is programmed to the board.

The range code does not apply to the S models, for the are always differenti al and bipolar. The *Frequency* and *ClockSource* ADC ActiveX control must be setup before calling the configure function.

EDREADX.Frequency

Frequency	The ADC sampling frequency

WARNING!!

- On the PCI703 the frequency is the update rate of the A/D converter. This means that the board will convert the channels at a period of equal to the frequency and the channels in the sequence of the channel list. The end result is that the time between samples is equal to 1/Frequency.
- The PCI703S -frequency relates to th e total sampling frequency. The effective sampling frequency is the *frequency* divided by the channel list length. The channel-list holds all the channels that need to be simultaneous -sampled-and-holded. Thus the all channel in a set are sampled at the same time but the space between a set is the total sampling frequency divided by the channel list length. Also note that the sample-and-hold counts as one channel. This reduces the maximum frequency by one count plus the channel list length. For example the max for one channel is 200KHz.

Frequency Example:

PCI703	PCI703S
Frequency = 200 000 Hz Channel List Length = 10 Time = 5 uS Time between channels = 5 uS	Frequency = 200 000 Hz Channel List Length = 10 Effective Frequency = 20 000 Hz Time = 50 uS Time between channels = 0 uS Time between sets = 50 uS

EDREADX.ClockSource

ClockSource

This parameter is used to configure the clocking system of the ADC.
Format

Offset (bits)	Description
0	Clock Source (C0-C7) 0: Undefined 1: Internal 2: External
8	Trigger Source (T0-T3) 0: Internal 1: Reference (NOT SUPPORTED BY PCI 703S) 2: External
12	Trigger Mode – Only applies to the reference trigger source. (M0-M3) 0: Positive 1: Negative 2: Rising 3: Falling

Example Layout:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M3	M2	M1	M0	T3	T2	T1	T0	C7	C6	C5	C4	C3	C2	C1	C0

Starting and Stopping the ADC process

A single call is necessary to start or stop the ADC process

API-CALL
Long EDRE_ADStart (ulng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Start ()

Parameter	Type	Description
Return	Long	Error Code

API-CALL
Long EDRE_ADStop (ulng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Stop ()

Parameter	Type	Description
Return	Long	Error Code

Getting data from the driver buffer

A single call is necessary copy data from the driver buffer to the user buffer.

API-CALL
Long EDRE_ADGetData (ulng Sn, plong Buf, pulng BufSize)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to an unsigned long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.GetData (plong Buffer, plong Size)

Parameter	Type	Description
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to a long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

Querying the ADC subsystem

The driver can be queried to check the status of the ADC subsystem. The number of unread samples is one example.

API-CALL
Long EDRE_Query (ulng Sn, ulng QueryCode, ulng Param)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
QueryCode	Unsigned long	Query code. See appendix Example: ADUNREAD: This will tell you the number of available samples. ADBUSY: Is the ADC subsystem busy?
Param	Unsigned long	Extra parameter.
Return	Long	Returned query code

ACTIVEX CALL
Long EDREADX.GetUnread ()

Parameter	Type	Description
Return	Long	Number of samples available in the driver.

This function automatically queries the ADC driver buffer for the number of available samples.

Query Codes

This chapter explains query codes and their functions relating to the PCI703 series. It will show examples of typical query codes that can make custom application allot easier to develop and tailor made for the PCI703 boards. Please note that all examples or pseudo code will show the API call and not the ActiveX call. Use the section below to translate between the two different implementations.

How to use query codes

The appendix shows a list of query code that can be used. The function prototypes below show how to implement a query code for both the EDR Enhanced API and Utility ActiveX control.

API Call

Long EDRE_Query (ulng Sn, ulng QueryCode, ulng Param)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
QueryCode	Unsigned long	Query code. See appendix Example: ADUNREAD: This will tell you the number of available samples. ADBUSY: Is the ADC subsystem busy?
Param	Unsigned long	Extra parameter.
Return	Long	Returned query code

ActiveX Call

Long EDREUTLX.Query (long Code, long Param)

Parameter	Type	Description
Code	Unsigned long	Query code. See appendix
Param	Unsigned long	Extra parameter.
Return	Long	Returned query code

The above functions are used to execute query codes that can do a variety of functions. The returned value will have the result of the query code. The query function can also execute functions or changes settings of the driver system.

How to change the hardware FIFO depth

The hardware FIFO depth can be set with a single query call. This also relates to the interrupt depth and data update rate. If sampling at maximum speed set this depth to max and for slower speeds, under a 1000 Hz to a lower level.

PSEUDO BEGIN

*UI32 Sn=1000000001 /*32-bit unsigned integer - Serial Number*/*
*UI32 Depth=1000 /*32-bit unsigned integer - FIFO Depth, Max is 4095*/*
*I32 Status /*32-bit integer*/*

*Status=EDRE_Query(Sn, ADIRQLEVEL /*Code 142*/,Depth)*
If Status < 0 Then Error

PSEUDO END

How to check for available data

To check for the number of samples available in the driver buffer use the query functions as below.

PSEUDO BEGIN

*UI32 Sn=1000000001 /*32-bit unsigned integer - Serial Number*/*
*I32 Status /*32-bit integer*/*

*Status=EDRE_Query(Sn, ADUNREAD /*Code 109*/,0)*
If Status < 0 Then Error
Print "Samples available = " + Status

PSEUDO END

How to get the driver buffer size

To get the driver buffer size, use the query below.

PSEUDO BEGIN

*UI32 Sn=1000000001 /*32-bit unsigned integer - Serial Number*/*
*I32 Status /*32-bit integer*/*

*Status=EDRE_Query(Sn, ADBUFFSIZE/*Code 106*/,0)*
If Status < 0 Then Error
Print "Driver buffer size = " + Status

PSEUDO END

How to get the number of ADC channels

To check for the number of ADC channels

PSEUDO BEGIN

*UI32 Sn=1000000001 /*32-bit unsigned integer - Serial Number*/*
*I32 Status /*32-bit integer*/*

*Status=EDRE_Query(Sn, ADNUMCHAN /*Code 100*/,0)*
If Status < 0 Then Error
Print "Channels available = " + Status

PSEUDO END

How to check the status of the driver buffer

The driver buffer can be queried to check if a overrun condition occured.

PSEUDO BEGIN

*UI32 Sn=1000000001 /*32-bit unsigned integer - Serial Number*/*
*I32 Status /*32-bit integer*/*

*Status=EDRE_Query(Sn, ADBUFFOVER/*Code 107*/,0)*
If Status = 0 Then Print "Buffer OK"
Else Print "Buffer Error"

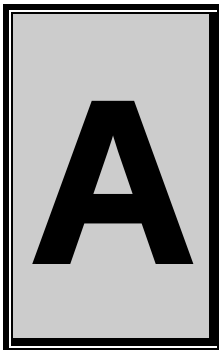
PSEUDO END

5. Calibration

Calibrating the PCI703 is simple task. EDR Enhanced must be installed and the calibration software. Both can be found on the Eagle Technology Software CD-Rom (*<EAGLECD>\EDRE\APPS\PCI700CAL\PCI700CALIBRATIONSOFTWARE.EXE*). The latest version will also be available on http://www.eagle.co.za.

Requirements

1. 1 x PCI703 with cable and adaptor.
2. Installed software
3. High accuracy calibration source,
4. High accuracy digital voltmeter.



A. Specifications

Maximum Transfer Bandwidth – PCI703/S

The ADC and DAC subsystems share a common data path to the FIFO module. This limits the maximum data transfer between the FIFO's, the appropriate device and across PCI. The maximum bandwidth is 450 000 cycles per second.

Analog Input Characteristics – PCI703

Input Characteristics

Input Signal Ranges

Channel Gain	Unipolar Range	Bipolar Range
0.25	0-10V	±10V
0.50	0-10V	±5V
1.00	0-5V	±2.5V
2.50	0-2V	±1V
5.00	0-1V	±500 mV
10.00	0-500mV	±250 mV
25.00	0-200mV	±100 mV
50.00	0-100mV	±50 mV
100.00	0-50mV	±25 mV

Input Coupling DC
Maximum Working Voltage ±11V relative to analog ground
Over Voltage Protection ±25V when power is on, relative to analog ground
±35V when power is off, relative to analog ground
FIFO Buffer Size 4096
Channel List Buffer Size Maximum 2048
Data Transfer Programmed I/O, Interrupts, BM DMA

Conversion Characteristics

Maximum Sampling Rate 400 000 samples per second (S/s)
Resolution 14 bits
Relative Accuracy ±1 LSB max
Offset Error (Gain = 1) ±0.4 mV max
Offset Error (Gain = 10) ±0.6 mV max
Offset Error (Gain = 50) ±0.1 mV max
Gain Error ±0.02% of max reading

Differential Input Amplifier Characteristics (AD620BR)

Input Impedance 10 GΩ , in parallel with 100 pF maximum
Bandwidth 600 KHz
Settling Time 5 uS to 2 LSB
15 uS to 1 LSB
System Noise Gains < 5, 0.6 LSB (rms)

	Gains > 5, 0.8 LSB (rms)
Maximum Safe Input Range	±15V
Maximum Operating Input Range	±5V

Analog Input Characteristics – PCI703S

Differential Input Amplifier Characteristics (AD620BR)

Input Coupling	DC
Input Impedance	>1 GΩ , in parallel with 50 pF maximum
Bandwidth	120 KHz at ± 5V input voltage swing
Offset Voltage	± 500 uV
Gain Error	± 0.002% (Gain=1)
Maximum Safe Input Range	±15V
Maximum Operating Input Range	±5V

Sample and Hold Amplifier Characteristics (AD684)

Bandwidth	1 MHz at ± 5V input voltage swing
Hold Mode Offset Voltage	± 3 mV
Gain Error	± 0.05%

Programmable Gain Amplifier Characteristics

Bandwidth	600 KHz at ± 5V input voltage swing
Offset Voltage	± 200 uV
Gain Error	± 0.008%

Input Characteristics

Input Signal Ranges

Channel Gain	Bipolar Range
0.50	± 5V
1.00	±2.5V
2.50	± 1V
5.00	± 500 mV
10.00	± 250 mV
25.00	±100 mV
50.00	± 50 mV
100.00	± 25 mV

Input Coupling	DC
Maximum Working Voltage	± 10V relative to analog ground
Over Voltage Protection	± 25V when power is on, relative to analog ground ± 35V when power is off, relative to analog ground
FIFO Buffer Size	4096
Channel List Buffer Size	Maximum 2048
Data Transfer	Programmed I/O, Interrupts, BM DMA

Conversion Characteristics

Maximum Sampling Rate	400 000 samples per second (S/s)
Resolution	14 bits
Relative Accuracy	± 1 LSB max
Offset Error (Gain = 1)	± 0.4 mV max
Offset Error (Gain = 10)	± 0.6 mV max
Offset Error (Gain = 50)	± 0.1 mV max
Gain Error	± 0.02% of max reading

Analog Output Characteristics

Output Characteristics

Resolution	14 bits
Maximum Update Rate	400 KHz to 0.02% full scale
FIFO Buffer Size	4096
Data Transfer	Programmed I/O, Interrupts, BM DMA

Conversion Characteristics (Calibrated)

Resolution	14 bits
Relative Accuracy	±1.0 LSB max
Full Scale Error	±0.9 LSB
Zero Scale Error	±0.9 LSB

Voltage Output Characteristics

Range	±10 Volt
Output Settling Time	2.5 us to 0.02% full scale
Output Impedance	0.2 Ω
Output Drive	±5 mA
Power-on State	0V

Digital Input/Output Characteristics

Number of Channels 8 independent programmable
Compatibility TTL
I/O Characteristics

Level	Min	Max
Input Low Voltage	0V	0.8V
Input High Voltage	2.0V	5.25V
Low Level Input Current		- 100 uA
High Level Input Current		100 uA
Output High Voltage	2.4V	
Output Low Voltage		0.6V
Low Level Output Current		-24 mA
High Level Output Current		4mA

Multifunction Input/Output Characteristics

Number of Channels 10 independent programmable
Compatibility TTL
I/O Characteristics

Level	Min	Max
Input Low Voltage	0V	0.8V
Input High Voltage	2.0V	5.25V
Low Level Input Current		- 100 uA
High Level Input Current		100 uA
Output High Voltage	2.4V	
Output Low Voltage		0.6V
Low Level Output Current		-24 mA
High Level Output Current		4mA

Timing Input/Output Characteristics

Number of Channels 2
Resolution 24 bits
Clock Source 20 MHz, 100 KHz, External
I/O Characteristics

Level	Min	Max
Input Low Voltage	0V	0.8V
Input High Voltage	2.0V	5.25V
Low Level Input Current		- 100 uA
High Level Input Current		100 uA
Output High Voltage	2.4V	
Output Low Voltage		0.6V
Low Level Output Current		-24 mA
High Level Output Current		4 mA

Other

Bus Interface PCI 2.2 Compatible
Master & Slave
3.3V or 5V
Power Requirements +5V (±5%) @ 1.3 A

B

B. Configuration Constants

Query Codes

Please see the file <EAGLECD>\EDRE\INCLUDE\QUERY.H for the latest query codes.

Error Codes

Please see the file <EAGLECD>\EDRE\INCLUDE\ERRORS.H for the latest error codes.

Digital I/O Codes

Name	Value	Description
DIOOUT	0	Port is an output.
DIOIN	1	Port is an input.
DIOINOROUT	2	Port can be configured as in or out.
DIOINANDOUT	3	Port is an input and an output.

Analog Input Gain Codes – PCI703-16/32/64/A

Name	Value	Description
GAIN 0.25	0	Gain of ¼ (±10V, NU)
GAIN 0.50	1	Gain of ½ (±5V, 0-10V)
GAIN 1.00	2	Gain of 1 (±2.5V, 0-5V)
GAIN 2.50	3	Gain of 2.5 (±1V, 0-2V)
GAIN 5.00	4	Gain 0f 5 (±500mV, 0-1V)
GAIN 10.0	5	Gain of 10 (±250mV, 0-500mV)
GAIN 25.0	6	Gain of 25 (±100mV, 0-200mV)
GAIN 50.0	7	Gain of 50 (±50mV, 0-100mV)

Analog Input Gain Codes – PCI703S-8/16/A

Name	Value	Description
GAIN 0.50	0	Gain of ½ (±5V)
GAIN 1.00	1	Gain of 1 (±2.5V)
GAIN 2.50	2	Gain of 2.5 (±1V)
GAIN 5.00	3	Gain 0f 5 (±500mV)
GAIN 10.0	4	Gain of 10 (±250mV)
GAIN 25.0	5	Gain of 25 (±100mV,)
GAIN 50.0	6	Gain of 50 (±50mV)
GAIN 100.0	7	Gain of 100 (±25mV,)

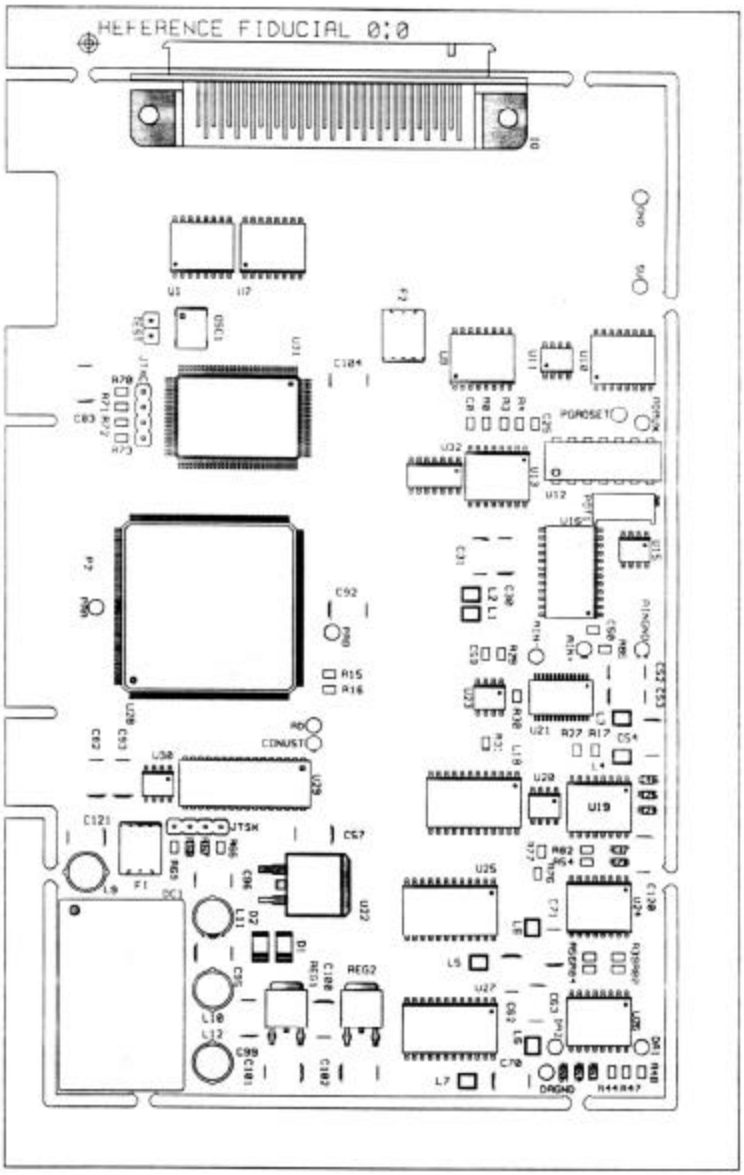
Analog Input Range Codes – PCI703-16/32/64/A

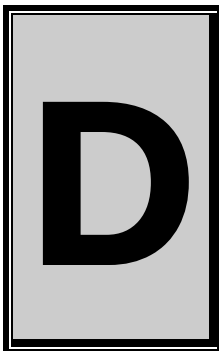
**The range code does no apply to the S-models for they are always in differential bipolar mode.*

Name	Value	Description
UNIPOLAR, SINGLE ENDED	0	Channel is single ended unipolar input.
BIPOLAR, SINGLE ENDED	1	Channel is single ended bipolar input.
UNIPOLAR, DIFFERENTIAL	2	Channel is differential unipolar input.
BIPOLAR, DIFFERENTIAL	3	Channel is differential bipolar input.

C

C. Layout Diagram





D. Ordering Information

For ordering information please contact Eagle Technology directly or visit our website www.eagle.co.za. They can also be emailed at eagle@eagle.co.za.

Board	Description
PCI 703-16	16 Channel analog input board
PCI 703-16A	16 Channel analog input and 2 channel analog output board
PCI 703-32	32 Channel analog input board
PCI 703-32A	32 Channel analog input and 2 channel analog output board
PCI 703-64	64 Channel analog input board
PCI 703-64A	64 Channel analog input and 2 channel analog output board
PCI 703S-8	16 Channel sample-and-hold analog input board
PCI 703S-8A	16 Channel sample-and-hold analog input board and 2 channel analog output board
PCI 703S-16	16 Channel sample-and-hold analog input board
PCI 703S-16A	16 Channel sample-and-hold analog input board and 2 channel analog output board

Table D-D-1 Ordering Information

Please visit our website to have a look at our wide variety of data acquisition products and accessories.